Docket No.: 61282-056 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Kenichi TAJIKA, et al.	:	Confirmation Number:
Serial No.:	:	Group Art Unit:
Filed: January 30, 2004	:	Examiner:

For: CLOCK DELAY ADJUSTING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE FORMED BY THE METHOD

CLAIM OF PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. 119, Applicants hereby claim the priority of:

Japanese Patent Application No. 2003-024093, filed January 31, 2003
and
Japanese Patent Application No. 2003-313917, filed September 5, 2003

cited in the Declaration of the present application. Certified copies will be filed in due course.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:prg
Facsimile: (202) 756-8087
Date: January 30, 2004